3D-ICs: Advances in the Industry

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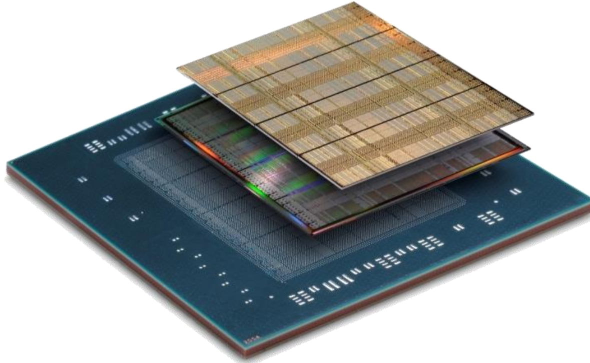
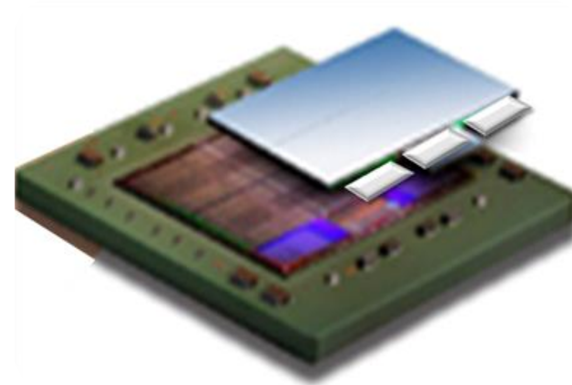
Outline

- 3D IC Background
- 3D IC Technology Development
- Summary
- Acknowledgements





Stacked ***S***ilicon ***I***nterconnect ***T***echnology refers to Xilinx 3D solutions

3D IC Background

Technical Challenges & Costs Are Growing

Our visibility always ~10 yrs – need broad exploration

TECHNOLOGY GENER

45nm	32nm	22
2007	2009	20

MANUFACTURING DEVELO

Not t

- Silicon lattice is ~ 0.5nr
10 latti

IBM Systems and Technology Group

Is there a Problem ?

Pricing: X'over on Transistor Cost

45 nm	32 nm	22 nm	14 nm	10 nm
Immersion (ArFi)	2nd Generation Immersion	3rd Gen ArFi w/ Source Mask Optimization (SMO)	4th Gen ArFi w/ SMO & Double Patterning (DPL)	5th Gen ArFi w/ Multilayer Patterning or EUV

- Process Complexity has increased node to Node
  (This is not atypical)
  But ....
- Technical barriers have precluded new Lithographic solutions such as EUV
- This leads to extremely complex patterning solutions
- Net: neither per wafer nor per gate showing historical cost reduction trends

Normalized cost (to 90nm)

Litho node (nm)

3 GSA Silicon Summit 2012 (S.S. Iyer)

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- Process Technology Path Below 10nm is unclear
- Cost Reduction Slowing from Complexity / Investment Increases
- Cost Per Wafer & Cost Per Gate Deviating from Historical Reduction

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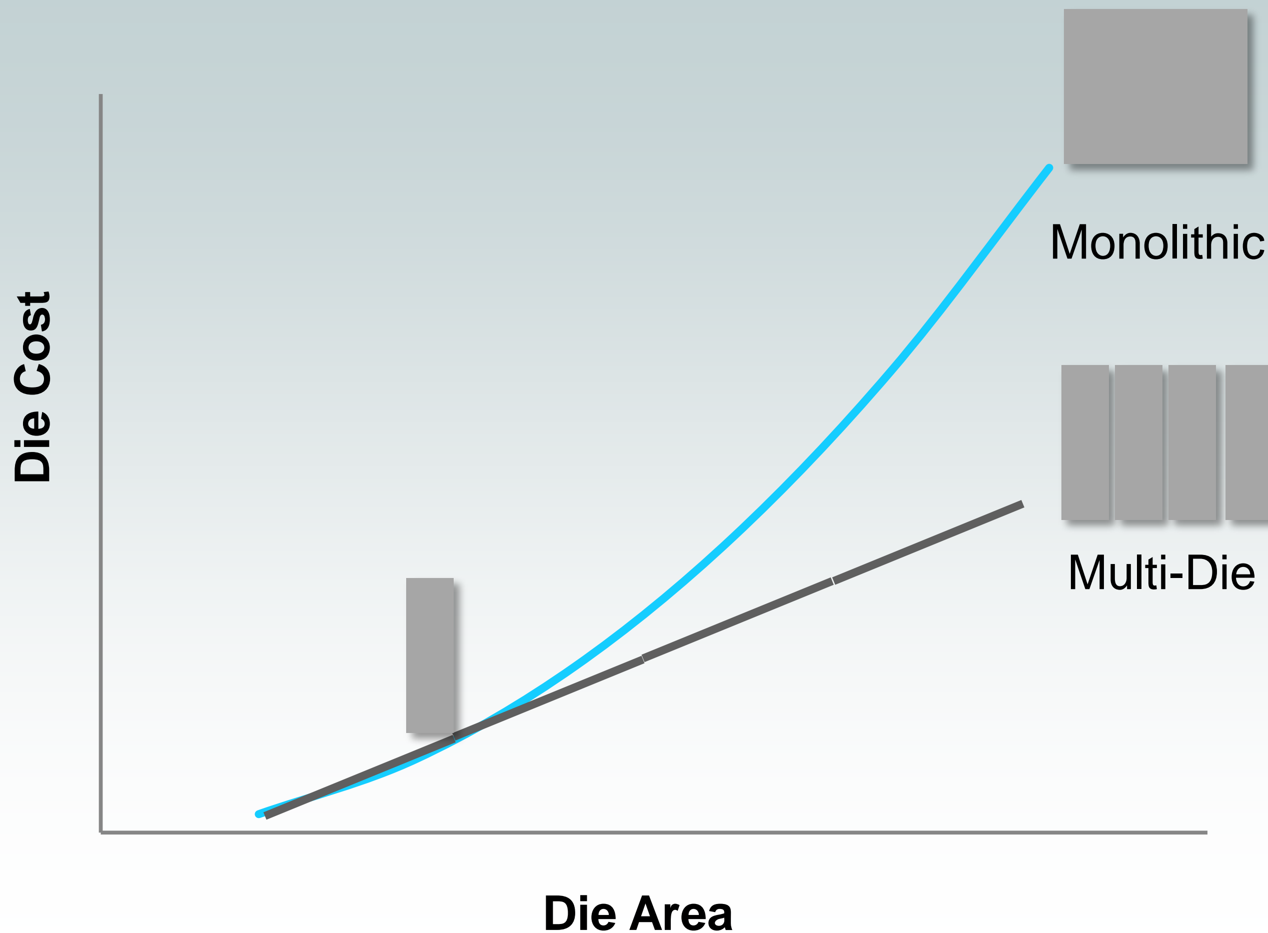
3DIC Extends Moore's Law
Cost Comparison: Monolithic vs. Multi-Die

"Moore's Law is Really About Economics" *– Gordon Moore*



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Design Rule Comparison

Design Rules for Die to Die interconnection	MCM (Substrate)	MCM with Silicon Bridge	Silicon Interposer (65 nm BEOL)	WLFO / Organic Interposer
Minimum Bump pitch (um)	150 (C4)	150 (C4) 40 (u-bump) bridge	< 40 (u-bump)	40 um RDL pad pitch
Via size / pad size (um)	60 / 90	0.4 / 0.7	0.4 / 0.7	10/30
Minimum Line & Space (um)	15 / 15	0.4 / 0.4	0.4 / 0.4	3 / 3
Metal thickness (um)	10	1	1	2-5
Dielectric thickness (um)	30	1	1	< 5
# of die-to-die connections per layer + GND shield layer (2L)	100's	10,000's	10,000's	1000's
Minimum die to die spacing (um)	4000	Bridge ~ 2500	150	< 250
# of High density layers feasible	Not a limitation	Not a limitation	Not a limitation	1-3L layers
Die Sizes for assembly and # of assemblies	Not a concern	Size & # limitation?	Not a concern	Size limitation?

- **Xilinx pursuing Silicon Interposer for design rule density, BW and lower power – e.g. die partition**

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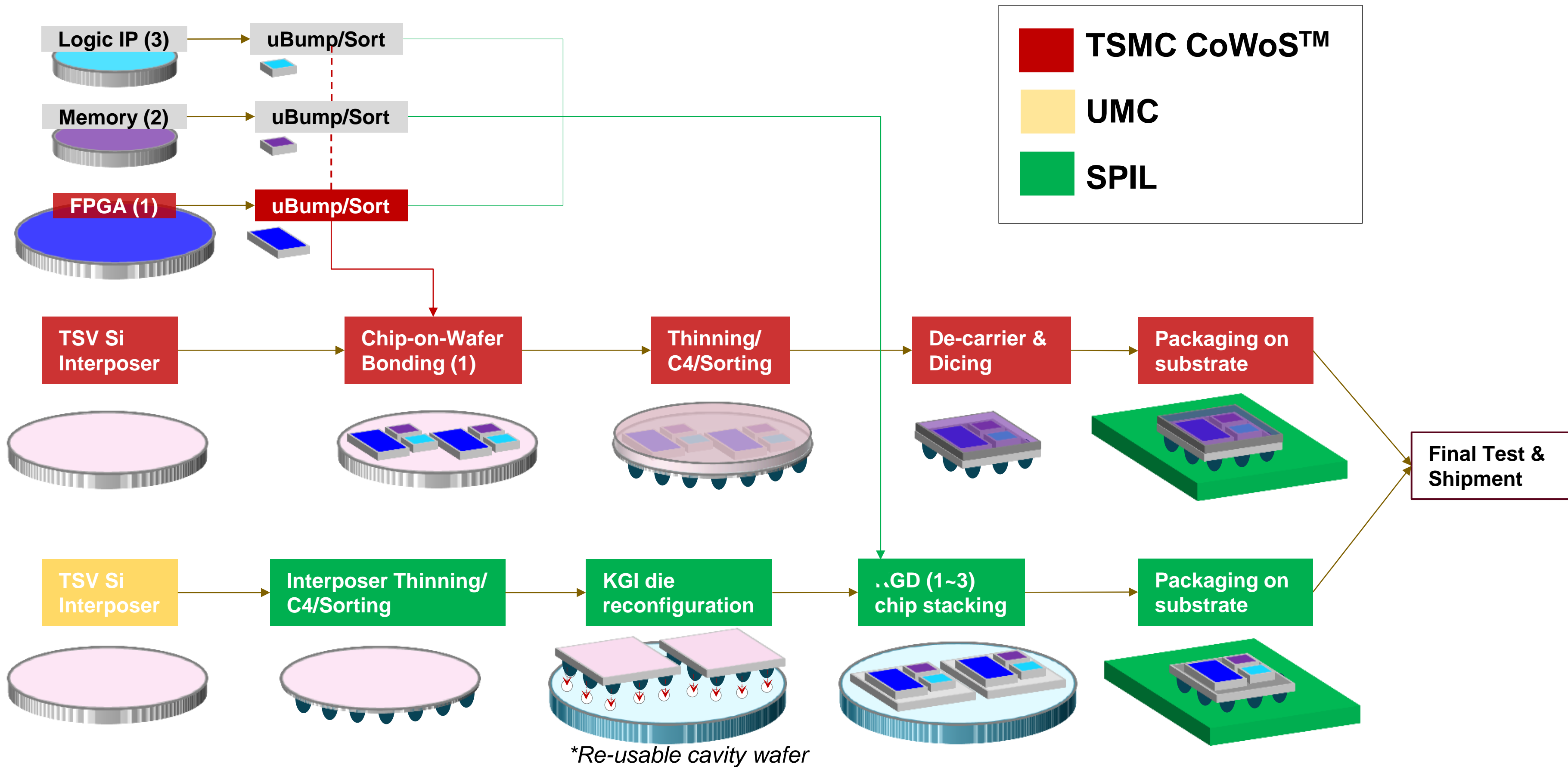
Supply Chain

- TSMC CoWoS in production
- Readying UMC/SPIL as additional source. Completed technology qualification



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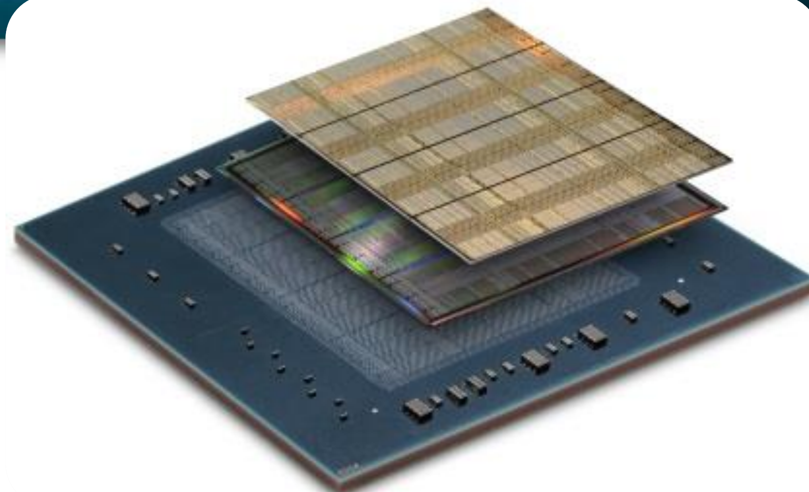
Xilinx 28nm 3DIC – Huge Leap in Innovation

Earth

Area: ~500 Million km^2

Population: ~6.8 Billion People

Oceans: 5



Virtex-7 2000T

Interposer Area: ~775 mm^2

Population: ~6.8 Billion Transistors

Chips: 5

- **136 Patents Awarded Worldwide**
- **226 Pending Applications Worldwide**

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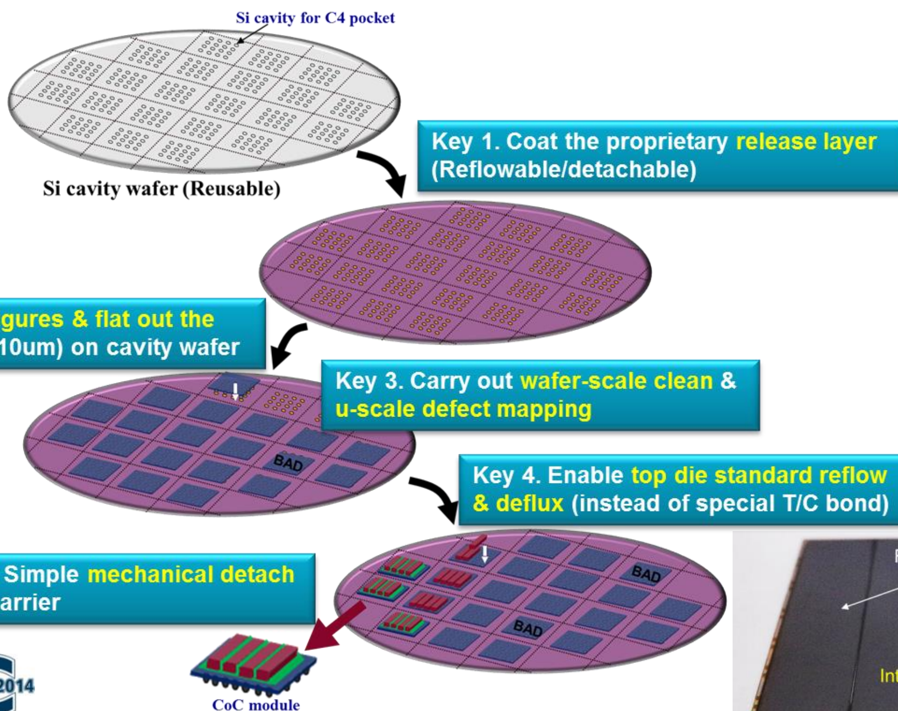
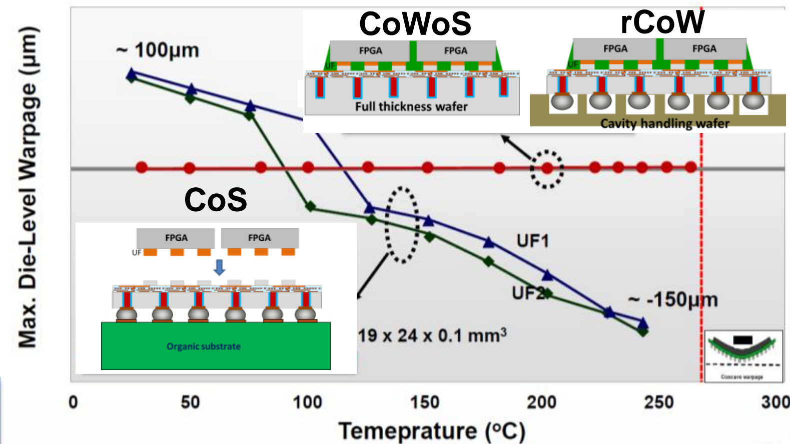
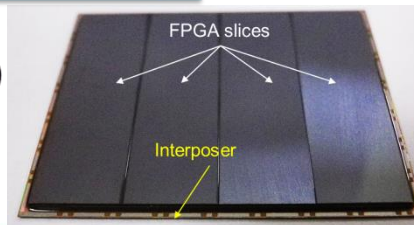
3D IC Technology Development

Critical Challenge: Warpage Control

- **CoWoS Technology**
  - Top dies are attached to full-thickness interposer wafers thus getting around the thin interposer warpage and poor micro-bump joining problem
- **Reconfigurable CoW (rCoW) Technology**
  - Xilinx patent issued worldwide (US/TWN/CN/EU/IND/JPN/KR)
  - Release layer approach that withstands reflow & maintains low warpage







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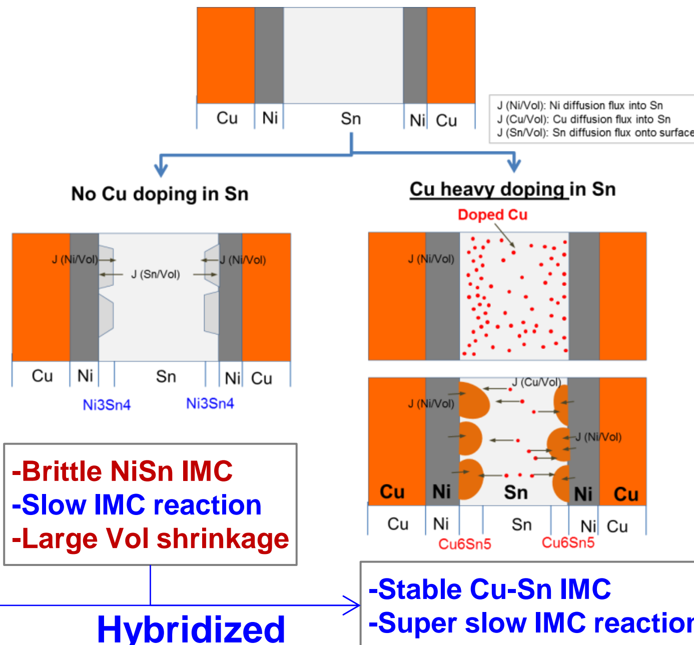
HTS Aging Reliability Issue

- **Voiding or crack in micro-joint during long term stress (HTS in particular)**
  - Due to limited Sn source and its dual consumption rate from top and bottom pad.
- **Resolution : Heavy Cu doping into LF solder cap (with Ni barrier layer)**
  - Take advantages of ductile IMC (Cu-Sn) and slower IMC reaction (Ni with Cu-Sn IMC)
  - Passed 3X reflow + 150°C aging condition for > 1000 hrs
  - **Xilinx X-4281 patent pending**

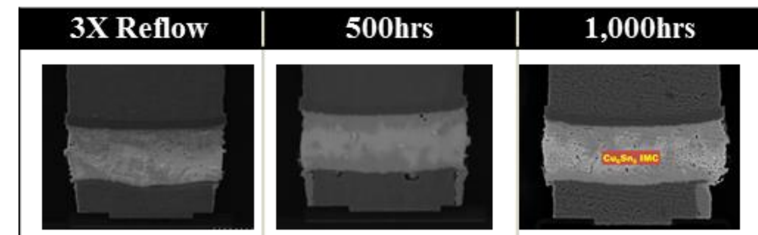
Diffusion flux model of inter-diffusion

Standard Cu/Solder

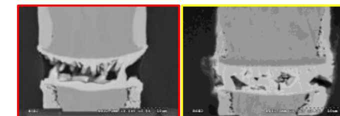
-Fast Cu-Sn reaction
-kirkendal void form
-Ductile IMC



HTS aging performance



*Reference images
(from no-doping u-bump)



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3D IC Technology Landscape

	Chip level	Device level	W2W C2W level
Players	**Samsung** DRAM / **Hynix** NAND & DRAM / **IBM** / **Micron** / **Elpida** / **Qualcomm** / **Nokia**	**Samsung** Vertical-Gate NAND/ **Besang** / Monolithic 3D IC / Stanford	**SONY (Stacked CIS)** / **Tezzaron** / Ziptronix/ MIT Lincon Lab
TSV size	5~10um	0.5~2um contact through oxide	2~5um in diameter
TSV pitch	30~50um	1~4um (not limited)	5~10um
TSV count	1k~5k	Not limited	Not limited
Key features			

Fig. 4 By moving the high-voltage transistors needed for anti-fuse programming underneath the 3D structure, FPGAs with densities comparable to ASICs can be stacked in a 3D format without the need for TSVs, according to NuPGA Corp. (courtesy of NuPGA Corp.)

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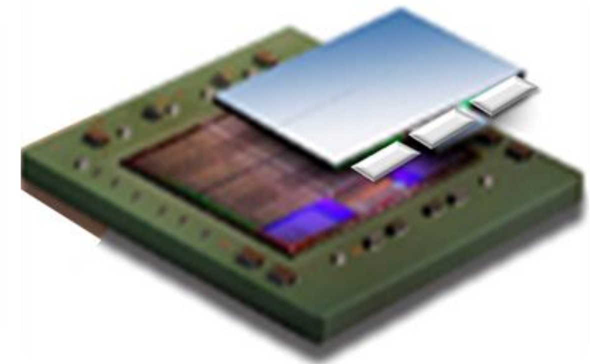
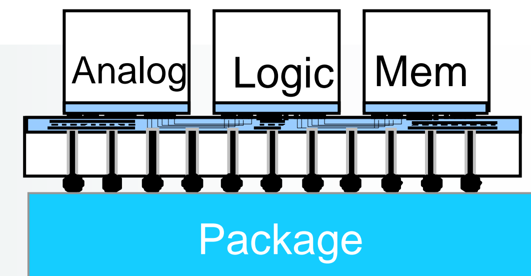
Summary

STACKONOMICS

- Economic and technology forces are aligned to enable 2.5D/3D stacking



- TSV and 3D stacking already deployed in Smartphones, High end FPGAs & Servers



- The “end game” will see three distinct technologies: Logic, Memory, Analog

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Acknowledgements

- **Xilinx**
  - R&D, NPI & Operation Teams
- **Partners**
  - TSMC R&D and Production Teams for FPGA, CoWoS
  - UMC for Interposer
  - SPIL R&D for MEOL and Advanced Packaging
  - Fujitsu Interconnect Technology for High Speed Substrates